US-PAT-NO: 5638534

DOCUMENT-IDENTIFIER: US 5638534 A

TITLE: Memory controller which executes read and write commands out of order

DATE-ISSUED: June 10, 1997

US-CL-CURRENT: 711/158, 711/105 , 711/167

APPL-NO: 08/ 415038

DATE FILED: March 31, 1995

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Brief Summary Text - BSTX (9):

Systems utilizing the posted write feature include logic to compare read addresses with write addresses to make sure that a subsequent read from the memory system is not directed to a memory address which has posted write data which have not already been written. If the read address corresponds to a posted write address, the memory controller may wait to respond to the read request until the posted write operation is completed, or, in the alternative, the memory controller may respond to the read request by transmitting data directly from the posted write buffer. If the read address is different from the addresses of all the posted writes, the memory controller may include "read-around" logic to enable the memory controller to respond to the read access to a different location before completing the posted write operations.

Brief Summary Text - BSTX (10):

Known memory controllers which implement posted write operations operate on a first-in, first out basis. That is, the posted writes are written to memory in the same order in which the posted writes are received by the memory controller. If sequential posted write operations are directed to addresses in different pages of the DRAMs, the memory system incurs the time penalty caused by the row access time. Even if two posted writes in the buffer are directed to the same memory page, a conventional memory controller does not write the two posted writes in sequence if a third posted write directed to a different page is posted between them. Furthermore, if the memory controller permits read-around operations to occur, the read access may be from a different page than a previous posted write or a subsequent posted write. This will again cause the row access time penalty to be incurred. If the microprocessor cannot post further writes or has to wait for read data when the memory controller slows down because of frequent page switching, the overall system performance will be degraded.

Drawing Description Text - DRTX (9):

FIG. 8 illustrates a block diagram of a memory subsystem which incorporates a posted write buffer and memory controller in accordance with the present invention.

Detailed Description Text - DETX (16):

The time penalty may be more significant in a microprocessor-based system which permits posted writes to memory. As discussed above, in a system having posted writes, such as a system 180 illustrated in FIG. 7, the microprocessor 113 applies an address, write data and appropriate control signals to the

system bus 125 to initiate a write access to the memory subsystem 120. Rather than wait for the completion of the write access, as indicated by the activation and subsequent deactivation of a busy signal from the memory subsystem 120, the microprocessor 113 continues issuing bus transactions. In order to accommodate posted writes, a memory controller 182 in the memory subsystem 180 includes it posted write buffer 184. The posted write buffer 184 stores the address and the data to be written to the DRAMs 135. In known posted write systems, the posted write buffer 184 may include storage for more than one posted write and operates as a first-in/first-out (FIFO) buffer. The memory controller 182 transfers the earliest posted write data to the DRAMs 135 by applying the address on the output of the posted write buffer 184 to the DRAMs as a row address portion and a column address portion as described above, with the difference that the address and data are provided by the posted write buffer 184 rather than directly from the system bus 125. The timing for storing write access request information into the FIFO buffer 184 and for applying the address and data outputs from the FIFO buffer 184 to the DRAMs 135 is provided by a timing generator and FIFO controller 186 via a control bus 187. The timing generator and FIFO controller 186 controls a row/column address multiplexer (MUX) 188 similar to that described above.

Detailed Description Text - DETX (17):

Generally, when the microprocessor 113 initiates a read access to the memory subsystem 120, the microprocessor 113 needs to have the responsive data before it continues with its next operation. Thus, exemplary posted write memory systems provide a read-around mode in which the memory controller 182 gives a read access request on the system bus 125 priority over pending posted writes. That is, if a read request is pending when a current access is completed, the read access is performed regardless of whether a posted write is pending, unless the read access request is directed to the same address location as a posted write. Because it is important that the read access retrieve the most current data, known posted write systems do one of two operations when a read request is directed to the same address as a posted write. The posted write buffer is flushed to write the write data to the DRAMs 135, or, alternatively, the read request is satisfied by outputting the requested data from the posted write buffer 184 in a similar manner to a cache memory subsystem. The read around mode is supported by a read/write address multiplexer (MUX) 190 which receives address information from the output of the posted write FIFO buffer 184 during write accesses and which receives address information directly from the system bus 125 during read accesses. A data output buffer 192 buffers the output dam from the DRAMs 135 onto the system bus 125.

Detailed Description Text - DETX (18):

Conventional posted write systems retain the time penalty when sequential posted writes are directed to different rows of the DRAMs 135. In particular, when the memory controller 182 accesses the FIFO posted write buffer 184, it must change the row address whenever two sequential posted writes are directed to different rows in the DRAMs 135. Furthermore, when a read access occurs on a row different from the row of the current access, the row access time penalty is incurred. A conventional memory controller partially reduces the time penalty by detecting when sequential addresses are directed to the same page (i.e., row). As illustrated in FIG. 7, a row latch and comparator 194 is included which receives the row address portion of the output of the read/write address multiplexer 190. The row latch and comparator 194 latches the row address portion of a previous access on occurrence of an active RAS* signal. The latched row address portion is compared with the row address portion of the current access to determine whether the two row addresses are the same. If the two row addresses are the same, the row latch and comparator 194 provides an active signal to the timing generator and FIFO controller to cause it to keep the current page (i.e., row) open and to change only the column address by generating the CAS* signal for the new current access.

Detailed Description Text - DETX (19):

FIG. 8 illustrates a memory subsystem 200 in accordance with the present invention. In particular, the memory subsystem 200 comprises a memory controller 202 which incorporates an improved posted write buffer 204. The memory controller 202 further includes a timing generator and buffer controller 206 which will be described in more detail below. The timing generator and buffer controller 206 is connected to the posted write buffer 204 via a bidirectional control bus 208.

Detailed Description Text - DETX (22):

Like the conventional posted write memory controllers, such as the one illustrated in FIG. 7, the timing generator in the posted write memory controller 202 of FIG. 8 keeps track of the row address of the current access via the row address latch 220. Unlike conventional memory controllers, the timing generator and buffer controller 206 includes comparison and pointer logic 230 which compares the row address portions of the currently open page (i.e., row) stored in the posted write buffer 204 and determines whether any of the active posted write requests has an address portion corresponding to the latched row address of the current access to the DRAMs 135. The comparison and pointer logic 230 further indicates the location within the posted write buffer 204 into which to store the address and data of incoming write, requests via an input pointer and indicates the location from which to output the address and data of a posted write selected as the next access to the DRAMs 135 via an output pointer.

US-PAT-NO: 6223301

DOCUMENT-IDENTIFIER: US 6223301 B1

TITLE: Fault tolerant memory

DATE-ISSUED: April 24, 2001

US-CL-CURRENT: 714/6

APPL-NO: 08/ 940282

DATE FILED: September 30, 1997

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Detailed Description Text - DETX (26):

To improve the data processing speed of the memory controller 12, the data buffer interface 52 also has a posted memory write (PMW) buffer 49. When a central processing unit (CPU) 20, for example, writes data to the memory 11, the CPU 20 waits for an acknowledgement from the memory controller 12. Because the write of data to the memory 11 may include at least two memory operations (i.e., require two clock cycles), the CPU 20 may be delayed in waiting for the acknowledgement. To prevent this from occurring, the controller 12 has a posted memory write (PMW) buffer 49 which acknowledges the completion of a write of the data to the memory modules 14 even though the write is still pending.

PGPUB-DOCUMENT-NUMBER: 20040064602

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040064602 A1

TITLE: Claiming cycles on a processor bus in a system having a PCI to PCI bridge north of a memory controller

PUBLICATION-DATE: April 1, 2004

US-CL-CURRENT: 710/22

APPL-NO: 10/ 262204

DATE FILED: September 30, 2002

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Detail Description Paragraph - DETX (16):

[0023] (a) for write cycles destined for the communications processing subsystem, the write data cannot be stalled with snoop stalls since the protocol allows request initiated data transfer to occur before snoop phase completion. The virtual bridge 18 is therefore configured to implement write posting buffers and will always be ready to accept data intended for it, once a write cycle is started (ADS # driven) and whenever the memory controller hub 40 is ready to accept a dummy write. The memory controller hub 40 is responsible for driving the TRDY #signal, but can ignore the data; and

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Inventor Name Search Result

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Last Name = JEDDELOH
First Name = JOSEPH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
11056273	Not Issued	020	02/11/2005	MEMORY MODULE AND METHOD HAVING ON-BOARD DATA SEARCH CAPABILITIES AND PROCESSOR-BASED SYSTEM USING SUCH MEMORY MODULES	JEDDELOH, JOSEPH M.
11056080	Not Issued	041	02/11/2005	MEMORY MODULE AND METHOD HAVING ON-BOARD DATA SEARCH CAPABILITIES AND PROCESSOR-BASED SYSTEM USING SUCH MEMORY MODULES	JEDDELOH, JOSEPH M.
11055528	Not Issued	019	02/10/2005	SYSTEM AND METHOD FOR CACHING DATA BASED ON IDENTITY OF REQUESTOR	JEDDELOH, JOSEPH
11041071	Not Issued	041	01/21/2005	MEMORY HUB BYPASS CIRCUIT AND METHOD	JEDDELOH, JOSEPH M.
10969331	Not Issued	020	10/19/2004	CALIBRATION OF MEMORY CIRCUITS	JEDDELOH, JOSEPH
10932473	Not Issued	030	09/01/2004	EMBEDDED DRAM CACHE MEMORY AND METHOD HAVING REDUCED LATENCY	JEDDELOH, JOSEPH
10839778	Not Issued	094	05/04/2004	METHOD OF IMPLEMENTING AN ACCELERATED GRAPHICS/PORT FOR A MULTIPLE MEMORY CONTROLLER COMPUTER SYSTEM	JEDDELOH, JOSEPH
10830872	Not Issued	041	04/23/2004	SYSTEM AND METHOD OF PROCESSING MEMORY REQUESTS IN A PIPELINED MEMORY CONTROLLER	JEDDELOH, JOSEPH
10776439	Not Issued	061	02/10/2004	ACCELERATED GRAPHICS PORT FOR A MULTIPLE MEMORY CONTROLLER COMPUTER SYSTEM	JEDDELOH, JOSEPH

10651021	Not Issued	094	08/27/2003	SYSTEM AND METHOD FOR CACHING DATA BASED ON IDENTITY OF REQUESTOR	JEDDELOH, JOSEPH
10601252	Not Issued	094	06/20/2003	MEMORY HUB AND ACCESS METHOD HAVING INTERNAL PREFETCH BUFFERS	JEDDELOH, JOSEPH
10464234	6745309	150	06/17/2003	PIPELINED MEMORY CONTROLLER	JEDDELOH, JOSEPH
10195779	6604180	150	07/11/2002	PIPELINED MEMORY CONTROLLER	JEDDELOH, JOSEPH
10123990	6853938	150	04/15/2002	CALIBRATION OF MEMORY CIRCUITS	JEDDELOH, JOSEPH
09971841	6789169	150	10/04/2001	EMBEDDED DRAM CACHE MEMORY AND METHOD HAVING REDUCED LATENCY	JEDDELOH, JOSEPH
09942389	6789155	150	08/29/2001	SYSTEM AND METHOD FOR CONTROLLING MULTI-BANK EMBEDDED DRAM	JEDDELOH, JOSEPH
09931728	6622228	150	08/16/2001	SYSTEM AND METHOD OF PROCESSING MEMORY REQUESTS IN A PIPELINED MEMORY CONTROLLER	JEDDELOH, JOSEPH
09908784	6449703	150	07/18/2001	PIPELINED MEMORY CONTROLLER	JEDDELOH, JOSEPH
09904632	6473817	150	07/13/2001	METHOD AND APPARATUS FOR EFFICIENT BUS ARBITRATION	JEDDELOH, JOSEPH
09892917	6717582	150	06/26/2001	ACCELERATED GRAPHICS PORT FOR A MULTIPLE MEMORY CONTROLLER COMPUTER SYSTEM	JEDDELOH, JOSEPH
09823602	Not Issued	071	03/30/2001	SERIAL PRESENCE DETECT DRIVEN MEMORY CLOCK CONTROL	JEDDELOH, JOSEPH
09805663	6636946	150	03/13/2001	SYSTEM AND METHOD FOR CACHING DATA BASED ON IDENTITY OF REQUESTOR	JEDDELOH, JOSEPH
09723403	6741254	150	11/27/2000	METHOD OF IMPLEMENTING AN ACCELERATED GRAPHICS PORT FOR A MULTIPLE MEMORY CONTROLLER COMPUTER SYSTEM	JEDDELOH, JOSEPH
09418468	6385680	150	10/15/1999	METHOD FOR FLEXIBLY ALLOCATING REQUEST/GRANT PINS BETWEEN MULTIPLE BUS	JEDDELOH, JOSEPH

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09418465	6389492	150	10/15/1999	APPARATUS FOR FLEXIBLY ALLOCATING REQUEST/GRANT PINS BETWEEN MULTIPLE BUS CONTROLLERS	JEDDELOH, JOSEPH
09201277	6085339	150	11/30/1998	SYSTEM FOR MEMORY ERROR HANDLING	JEDDELOH, JOSEPH
09173573	6363445	150	10/15/1998	METHOD OF BUS ARBITRATION USING REQUESTING DEVICE BANDWIDTH AND PRIORITY RANKING	JEDDELOH, JOSEPH
09173507	Not Issued	168	10/15/1998	APPARATUS FOR EFFICIENT BUS ARBITRATION	JEDDELOH, JOSEPH
09128410	6219765	150	08/03/1998	MEMORY PAGING CONTROL APPARATUS	JEDDELOH, JOSEPH
09127282	6295592	150	07/31/1998	METHOD OF PROCESSING MEMORY REQUESTS IN A PIPELINED MEMORY CONTROLLER	JEDDELOH, JOSEPH
09127207	6272609	150	07/31/1998	PIPELINED MEMORY CONTROLLER	JEDDELOH, JOSEPH
09121259	6363502	150	07/22/1998	METHOD FOR MEMORY ERROR HANDLING	JEDDELOH, JOSEPH
09108572	6052798	150	07/01/1998	SYSTEM AND METHOD FOR REMAPPING DEFECTIVE MEMORY LOCATIONS	JEDDELOH, JOSEPH
09000517	6157398	150	12/30/1997	METHOD OF IMPLEMENTING AN ACCELARATED GRAPHICS PORT FOR A MULTIPLE MEMORY CONTROLLER COMPUTER SYSTEM	JEDDELOH, JOSEPH
09000511	6252612	150	12/30/1997	ACCELERATED GRAPHICS PORT FOR MULTIPLE MEMORY CONTROLLER COMPUTER SYSTEM	JEDDELOH, JOSEPH
08928557	5953743	150	09/12/1997	METHOD FOR ACCELERATING MEMORY BANDWIDTH	JEDDELOH, JOSEPH
08903819	6035432	150	07/31/1997	SYSTEM FOR REMAPPING DEFECTIVE MEMORY BIT SETS	JEDDELOH, JOSEPH
08903818	5974564	150	07/31/1997	METHOD FOR REMAPPING DEFECTIVE MEMORY BIT SETS TO NON-DEFECTIVE MEMORY BIT SETS	JEDDELOH, JOSEPH

08887042	6049855	150	07/02/1997	A SEGMENTED MEMORY SYSTEM EMPLOYING DIFFERENT INTERLEAVING SCHEME FOR EACH DIFFERENT MEMEORY SEGMENT	JEDDELOH, JOSEPH
08887041	6202133	150	07/02/1997	METHOD OF PROCESSING MEMORY TRANSACTIONS IN A COMPUTER SYSTEM HAVING DUAL SYSTEM MEMORIES AND MEMORY CONTROLLERS	JEDDELOH, JOSEPH
08887039	5991855	150	07/02/1997	LOW LATENCY MEMORY READ WITH CONCURRENT PIPELINED SNOOPS	JEDDELOH, JOSEPH
08886908	6018792	150	07/02/1997	APPARATUS FOR PERFORMING A LOW LATENCY MEMORY READ WITH CONCURRENT SNOOP	JEDDELOH, JOSEPH
08859894	5935233	150	05/21/1997	COMPUTER SYSTEM WITH A SWITCH INTERCONNECTOR FOR COMPUTER DEVICES	JEDDELOH, JOSEPH
08815817	5950229	150	03/12/1997	SYSTEM FOR ACCELERATING MEMORY BANDWIDTH	JEDDELOH, JOSEPH
08767180	6076182	150	12/16/1996	MEMORY FAULT CORRECTION SYSTEM AND METHOD	JEDDELOH, JOSEPH
08744958	5933852	150	11/07/1996	SYSTEM AND METHOD FOR ACCELERATED REMAPPING OF DEFECTIVE MEMORY LOCATIONS	JEDDELOH, JOSEPH
08742773	5905858	150	11/01/1996	SYSTEM AND METHOD FOR MEMORY ERROR HANDLING	JEDDELOH, JOSEPH
08741603	5862314	150	11/01/1996	SYSTEM AND METHOD FOR REMAPPING DEFECTIVE MEMORY LOCATIONS	JEDDELOH, JOSEPH

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Inventor Name Search Result

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Last Name = LEE
First Name = TERRY

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60536331	Not Issued	159	01/13/2004	INTELLIGENT ASSET MANAGEMENT FOR HYBRID ON-DEMAND ARCHITECTURE	LEE, TERRY
60496964	Not Issued	159	08/20/2003	IC-PROCESSED POLYMER LIQUID CHROMATOGRAPHY SYSTEM ON-A-CHIP AND THE METHOD OF MAKING IT	LEE, TERRY D.
60460019	Not Issued	159	04/03/2003	PROCESS AND APPARATUS FOR FILTERING FISH TANKS, AQUARIUMS AND THE LIKE	LEE, TERRY
60232024	Not Issued	159	09/12/2000	XML BASED API FOR COMMERCE PLATFORMS	LEE, TERRY
60114900	Not Issued	159	01/05/1999	POLYMER-BASED ELECTROSPRAY CHIPS FOR MASS SPECTROMETRY	LEE, TERRY D.
60109264	Not Issued	159	11/19/1998	POLYMER BASED ELECTROSPRAY CHIPS FOR MASS SPECTROMETRY	LEE, TERRY D.
60055349	Not Issued	159	08/11/1997	SLDRAM ARCHITECTURE	LEE, TERRY
60036907	Not Issued	159	02/05/1997	DIELECTRIC SUPPORTED RADIO-FREQUENCY CAVITIES	LEE, TERRY G.
60036741	Not Issued	159	01/27/1997	MEMS ELECTROSPRAY NOZZLE FOR MASS SPECTROSCOPY	LEE, TERRY
29211210	D504910	150	08/10/2004	CRAYON WHEEL	LEE, TERRY
29042456	D378323	150	09/10/1995	PAINTBRUSH	LEE, TERRY
29009477	D351065	150	06/14/1993	PAINTBRUSH	LEE, TERRY
11153758	Not Issued	020	06/14/2005	APPARATUS AND METHODS FOR OPTICALLY-COUPLED MEMORY SYSTEMS	LEE, TERRY R.
11153722	Not	020	06/14/2005	APPARATUS AND METHODS	LEE, TERRY R.

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11152979	Not Issued	020	06/14/2005	APPARATUS AND METHODS FOR OPTICALLY-COUPLED MEMORY SYSTEMS	LEE, TERRY R.
11152978	Not Issued	020	06/14/2005	APPARATUS AND METHODS FOR OPTICALLY-COUPLED MEMORY SYSTEMS	LEE, TERRY R.
11059645	Not Issued	020	02/17/2005	TIMING CALIBRATION PATTERN FOR SLDRAM	LEE, TERRY R.
11045518	Not Issued	019	01/31/2005	METHOD AND APPARATUS USING FET SWITCHES FOR POINT TO POINT BUS OPERATION	LEE, TERRY R.
11035678	Not Issued	030	01/13/2005	INTELLIGENT ASSET MANAGEMENT IN A CABLE SERVICES SYSTEM	LEE, TERRY
11022594	Not Issued	020	12/22/2004	APPARATUS AND SYSTEM FOR MONITORING ENVIRONMENTAL FACTORS IN A COMPUTER SYSTEM	LEE, TERRY
11018384	Not Issued	020	12/22/2004	METHOD OF TIMING CALIBRATION USING SLOWER DATA RATE PATTERN	LEE, TERRY R.
10955625	Not Issued	077	09/30/2004	REMOVABLE COVER FOR AN ELECTRONIC DEVICE	LEE, TERRY
10954437	Not Issued	030	09/30/2004	MULTIPLE BATTERY ASSEMBLY FOR PORTABLE DEVICES	LEE, TERRY
10917257	Not Issued	030	08/11/2004	IC-PROCESSED POLYMER NANO-LIQUID CHROMATOGRAPHY SYSTEM ON-A-CHIP AND METHOD OF MAKING IT	LEE, TERRY D.
10692038	Not Issued	020	10/22/2003	SEMAPHORING SYSTEM BETWEEN SYSTEM FIRMWARE AND HARDWARE MANIPULATION SUBSYSTEM	LEE, TERRY
10648164	Not Issued	041	08/26/2003	VERTICAL SURFACE MOUNT ASSEMBLY AND METHODS	LEE, TERRY R.
10603573	Not Issued	030	06/24/2003	MICROFLUIDIC DEVICES AND METHODS WITH ELECTROCHEMICALLY ACTUATED SAMPLE PROCESSING	LEE, TERRY DWIGHT
10601253	Not	030	06/20/2003	POSTED WRITE BUFFERS AND	LEE, TERRY R.

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10601252	Not Issued	094	06/20/2003	MEMORY HUB AND ACCESS METHOD HAVING INTERNAL PREFETCH BUFFERS	LEE, TERRY R.
10601222	Not Issued	030	06/20/2003	SYSTEM AND METHOD FOR SELECTIVE MEMORY MODULE POWER MANAGEMENT	LEE, TERRY
10601104	Not Issued	041	06/19/2003	RECONFIGURABLE MEMORY MODULE AND METHOD	LEE, TERRY R.
10461207	Not Issued	030	06/12/2003	DYNAMIC SYNCHRONIZATION OF DATA CAPTURE ON AN OPTICAL OR OTHER HIGH SPEED COMMUNICATIONS LINK	LEE, TERRY R.
10458015	6837731	150	06/10/2003	LOCKING ASSEMBLY FOR SECURING A SEMICONDUCTOR DEVICE TO A CARRIER SUBSTRATE	LEE, TERRY R.
10436749	Not Issued	019	01/01/0001	DOOR KNOB PAINT COVERS	LEE, TERRY LYNN
10408540	6856567	150	04/07/2003	SEMICONDUCTOR DEVICE WITH SELF REFRESH TEST MODE	LEE, TERRY R.
10374449	6784367	150	02/25/2003	MICROELECTRONIC DEVICE ASSEMBLIES HAVING A SHIELDED INPUT AND METHODS FOR MANUFACTURING AND OPERATING SUCH MICROELECTRONIC DEVICE ASSEMBLIES	LEE, TERRY
10245229	Not Issued	041	09/16/2002	METHOD OF ALLOCATING MEMORY TO PERIPHERAL COMPONENT INTERCONNECT (PCI) DEVICES	LEE, TERRY PING-CHUNG
10173221	Not Issued	041	06/14/2002	METHOD AND DEVICE FOR PROVIDING COMPUTER SYSTEM COMPONENT DATA	LEE, TERRY
09991453	Not Issued	083	11/14/2001	METHOD OF ERROR ISOLATION FOR SHARED PCI SLOTS	LEE, TERRY PING-CHUNG
09649765	6548757	150	08/28/2000	MICROELECTRONIC DEVICE ASSEMBLIES HAVING A SHIELDED INPUT AND METHODS FOR MANUFACTURING AND	LEE, TERRY

				OPERATING SUCH MICROELECTRONIC DEVICE ASSEMBLIES	
09498359	6226134	250	02/04/2000	ADJUSTABLE MONOCULAR EYE SHIELD FOR TELESCOPES AND SIMILAR INSTRUMENTS	LEE, TERRY
09442843	Not Issued	041	11/18/1999	POLYMER-BASED ELECTROSPRAY NOZZLE FOR MASS SPECTROMETRY	LEE, TERRY D.
09017138	6025681	150	02/02/1998	DIELECTRIC SUPPORTED RADIO-FREQUENCY CAVITIES	LEE, TERRY G.
09013961	5994696	150	01/27/1998	MEMS ELECTROSPRAY NOZZLE FOR MASS SPECTROSCOPY	LEE, TERRY D.
08594542	5724846	150	01/31/1996	INTERRUPTION OF ROLLING MILL CHATTER BY INDUCED VIBRATIONS	LEE, TERRY C.
07107021	Not Issued	161	10/13/1987	PORTABLE RADIO INFORMATIONAL DEVICE	LEE, TERRY D.
05860710	4207290	150	12/15/1977	FLUE GAS SCRUBBER	LEE, TERRY J.

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